REMARKS

Claims 32, 34-51 and 58-62 are pending in the present application. Claims 32, 40 and 50-51 have been amended. Claim 33 has been canceled and its subject matter has been incorporated in amended independent claim 32. Claims 58-62 have been newly added to round out the scope of protection afforded by the present invention. No new matter has been introduced.

Claims 32-38 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Blatchford, Jr. et al. (U.S. Patent No. 6,200,734). This rejection is respectfully traversed.

Amended independent claim 32 recites "an integrated circuit comprising a reflective layer having a reflective surface, a first anti-reflective coating over the reflective surface, the first coating having a first index of refraction, a first absorption, a first thickness, and an upper surface defining a first interface, a second anti-reflective coating at least partially on the upper surface of said first anti-reflective coating, the second anti-reflective coating having a second index of refraction, a second absorption, a second thickness, and an upper surface defining a second interface, wherein the first index of refraction is different from the second index of refraction and the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coatings are chosen such that the amplitudes and phase differences of all sources of reflected radiation which reside at or below the second interface substantially mutually cancel when combined" (emphasis in original).

The device of Blatchford Jr. discloses a method of fabricating a semiconductor device that includes the step of forming an anti-reflection coating on a substrate having a non-polar surface. The anti-reflective coating includes at least two layers of a silicon-containing oxide having different ratios of silicon-to-oxide, which will produce different indices of refraction, and different extinction coefficients. The device of Blatchford Jr. fails to teach or suggest a first and second anti-reflective coating in which the indices of refraction, absorptions, and thicknesses of the first and second anti-reflective coatings are chosen such that the amplitudes and phase differences of all sources of reflected radiation

which reside at or below the second interface substantially mutually cancel when combined. Therefore, the rejection of claim 32 under 35 U.S.C. § 102(e) should be withdrawn.

Claims 34-38 depend from claim 32. Accordingly, the rejection of claims 34-38 under 35 U.S.C. § 102(e) should be withdrawn for at least the reasons given above with respect to claim 32.

Claim 39 stands rejected under 35 U.S.C. § 103(a) over Blatchford. This rejection is respectfully traversed. Claim 39 depends from claim 32 and is allowable at least for those reasons mentioned above in connection with claim 32, and because Blatchford Jr. does not teach, suggest, or otherwise motivate one skilled in the art to arrive at the respective inventive combination defined by claim 39. Accordingly, the rejection of claim 39 over Blatchford Jr. should be withdrawn.

Claims 40-45 and 47-50 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blatchford Jr. in further view of Fukuda et al. (U.S. Patent No. 6,255,151). This rejection is respectfully traversed.

Claim 40 recites *inter alia* a memory cell comprising a structure on a substrate, the structure comprising at least two active areas formed in the substrate, a first anti-reflective coating over the structure, the first anti-reflective coating adapted to stop an etch process and a second anti-reflective coating on at least a portion of the first anti-reflective coating, the second anti-reflective coating adapted to stop an etch process.

The device of Blatchford Jr. fails to teach or suggest an anti-reflective coating adapted to stop an etch process. The Office Action acknowledges that Blatchford Jr. fails to teach or suggest a specific type of semiconductor much less a memory cell comprising at least two active areas, a gate stack between the active areas and a capacitor in electrical contact with one of the active areas as taught in claim 40. In order to overcome these deficiencies in Blatchford Jr., the Office Action relies on Fukuda.

The device of Fukuda discloses a semiconductor integrated circuit device that

comprises memory cell selection MISFETs formed in a memory cell array region on a semiconductor substrate, peripheral circuit MISFETs formed in a peripheral circuit region around the memory cell array region, a first interlayer insulating film for covering the memory cell selection MISFETs and the peripheral circuit MISFETs, bit lines formed over the first interlayer insulating film lying in the memory cell array region, at least one information storage capacitive element provided with a lower electrode electrically connected to one source-to-drain region of each memory cell selection MISFET.

The device of Fukuda also fails to teach or suggest an anti-reflective coating adapted to stop an etch process. Thus, in light of the teachings of Fukuda, even if one accepts *arguendo* that Fukuda may be combined with Blatchford Jr., the proposed combination does not teach or suggest the invention as claimed. Accordingly, the rejection of claim 40 over Blatchford Jr. in view of Fukuda should be withdrawn.

Claims 41-45 and 47-49 depend from claim 40. Accordingly, the rejection of claims 41-45 and 47-49 under 35 U.S.C. § 103(a) should be withdrawn for at least the reasons given above with respect to claim 40.

Claim 50 recites an integrated circuit comprising *inter alia* at least one memory cell, the memory cell comprising an etch stop layer comprising a first anti-reflective coating over the structure, the first anti-reflective coating having a first index of refraction and a first absorption and a second anti-reflective coating on at least a portion of the first anti-reflective coating, the second anti-reflective coating having a second index of refraction and a second absorption.

The devices of Blatchford Jr. and Fukuda both fail to teach or suggest an etch stop layer comprising a first anti-reflective coating over the structure, the first anti-reflective coating having a first index of refraction and a first absorption and a second anti-reflective coating on at least a portion of the first anti-reflective coating, the second anti-reflective coating having a second index of refraction and a second absorption. Thus, in light of the teachings of Blatchford Jr. and Fukuda, even if one accepts *arguendo* that Fukuda may be combined with Blatchford Jr., the proposed combination does not teach or suggest the

invention as claimed. Accordingly, the rejection of claim 50 over Blatchford Jr. in view of Fukuda should be withdrawn.

Claim 46 stands rejected under 35 U.S.C. § 103(a) over Blatchford Jr. in view of Fukuda in further view of Figura et al. (U.S. Patent No. 6,025,624). Reconsideration and withdrawal of this rejection is respectfully requested.

The Office Action acknowledges that Blatchford Jr. and Fukuda fail to teach or suggest capacitors that are container capacitors. In order to overcome this deficiency, the Office Action relies on the combination of the Blatchford Jr. and Fukuda with Figura. However, the Examiner's use of Figura is not permitted to preclude patentability under 35 U.S.C. § 103(a) as provided by 35 U.S.C. § 103(c).

The present application was filed on September 1, 1999. Figura was filed on June 19, 1998 and issued on February 15, 2000. Figura thus qualifies as prior art under 35 U.S.C. § 102(e). In addition, the subject matter of Figura and the claimed invention were, at the time the invention was made, subject to an obligation of assignment to the same entity, that is Micron Technology, Inc. The Assignment for this application was recorded in the PTO on September 1, 1999, on Reel 010223, Frame 0705. The Assignee of Figura is shown on the face of the reference. Therefore, § 35 U.S.C. § 103(c) applies and, as a result, the Office Action's rejection of claim 46 based on the combination of the admitted Blatchford Jr. and Fukuda in view of Figura cannot be sustained and should be withdrawn.

Claim 51 stands rejected under 35 U.S.C. § 103(a) over Blatchford Jr. in view of Fukuda in further view of Podlesny et al. (U.S. Patent No. 5,724,299). Reconsideration and withdrawal of this rejection is respectfully requested.

Claim 51 recites a computer system comprising *inter alia* a processor and a memory, the memory comprising at least one memory cell, the memory cell comprising a first anti-reflective coating over the structure, the first anti-reflective coating having a first index of refraction and a first absorption and adapted to stop an etch process and a second anti-reflective coating formed on the first anti-reflective coating, the second anti-reflective

coating having a second index of refraction and a second absorption and adapted to stop an etch process.

As mentioned above with respect to claim 40, Blatchford Jr. and Fukuda fail to teach or suggest an anti-reflective coating adapted to stop an etch process. Podlesny discloses a multiport register file contains a storage element having first and second storage nodes, a plurality of first and second switched bit lines connecting to the first and second storage nodes, and at least one controlled supply line providing for switching on/off the storage element. Podlesny also fails to teach or suggest an anti-reflective coating adapted to stop an etch process.

Thus, in view of the teachings of Podlesny, and even if one accepts *arguendo* that Podlesny may be combined with Blatchford Jr. and Fukuda, the proposed combination does not teach or suggest the invention as claimed. Accordingly, the rejection of claim 51 over Blatchford Jr. and Fukuda in view of Podlesny should be withdrawn.

As noted, new claims 58-62 have been added to round out the scope of protection afforded the invention. New independent claims 60-62 each contain one or more patentable features of the invention emphasized in the above remarks.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By _____

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